Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1-8. (Canceled)

9. (Currently Amended) An apparatus comprising:

a processing engine to make enqueue requests;

a scheduler to make dequeue requests;

a cache memory to store data describing a structure of a queue;

a memory controller to initiate queue commands; and

a queue manager including a content addressable memory to store a reference to data in the cache memory describing the structure of the queue, the queue manager configured to process the enqueue requests and the dequeue requests and capable of commencing processing a request to a queue while a previous request with respect to the same queue is being processed,

wherein the cache memory is distributed partially to the memory controller and

wherein the queue manager is configured to issue commands to return data describing the structure of the queue and to fetch data describing an updated structure of the queue from memory to ensure that data describing the structure of the queue stored in the cache memory is coherent with entries in the content addressable memory.

10. (Previously presented) The apparatus of claim 9 further including memory to store data placed on a queue wherein the memory includes a linked list data structure.

11. (Original) The apparatus of claim 9 wherein the processing engine includes a plurality of multi-threaded pipelined programming engines, configured in a pipeline to receive, assemble, and classify data packets to determine an output queue for each packet and to make requests to the queue manager that specify the output queue.

12. (Original) The apparatus of claim 9 including a second plurality of multi-threaded pipelined programming engines, configured as a second pipeline to receive data from the queue manager and send data to a transmit buffer.

13. (Original) The apparatus of claim 9 wherein the scheduler includes multi-threaded pipelined programming engines, the scheduler configured to determine the order of packets to be removed from the queue and to store a bit for the queue indicating whether the queue is empty.

14. (Canceled)

15. (Currently Amended) A system comprising:

a source of data packets;

a destination of data packets; ~~and~~

a device operating to transfer data packets from the source to the destination comprising:

a processing engine to make enqueue requests;

a scheduler to make dequeue requests;

a cache memory to store data describing a structure of a queue;

a memory controller to initiate queue commands; and

a queue manager including a content addressable memory to store a reference to data in the cache memory describing the structure of the queue, the queue manager configured to process the enqueue requests and the dequeue requests and capable of processing a request to a queue while a previous request with respect to the same queue is being processed; and

a memory adapted to store a queue of buffers wherein the cache memory are distributed partially to the memory adapted to store a queue of buffers

wherein the ~~apparatus~~ device is connected to a high line rate, and

further wherein the cache memory is distributed partially to the memory controller.

16. (Previously presented) The system of claim 15 further including a memory to store data placed on a queue wherein the memory includes a linked list data structure.

17. (Original) The system of claim 15 wherein the processing engine includes a plurality of multi-threaded pipelined programming engines, configured in a pipeline to receive, assemble, and classify data packets to determine an output queue for each packet and to make requests to the queue manager that specify the output queue.

18. (Original) The system of claim 15 further including a second plurality of multi-threaded pipelined programming engines, configured as a second processing engine to receive data from the queue manager and send data to a transmit buffer.

19. (Original) The system of claim 15 wherein the scheduler includes multi-threaded pipelined programming engines, the scheduler configured to determine the order of packets to be removed from the queue and store a bit for each queue indicating whether the queue is empty.

20. (Original) The system of claim 15 wherein the queue manager is configured to issue commands to return data describing the structure of the queue and to fetch data describing an updated structure of the queue from memory to ensure that data describing the structure of the queue stored in the memory controller is coherent with the entries in the content addressable memory.

21-30. (Canceled)

31. (Previously presented) The apparatus of claim 9 wherein the cache memory are distributed partially to the queue manager.

32. (Previously presented) The apparatus of claim 9 further including a memory adapted to store a queue of buffers wherein the cache memory are distributed partially to the memory adapted to store the queue of buffers.

33. (Previously presented) The system of claim 15 wherein the cache memory are distributed partially to the queue manager.

34-35. (Canceled)